

Abstract of the DisclosurePACKET TRANSMISSION

The implementation of transactions on an integrated circuit comprising a plurality of functional modules connected to a packet router is described. Each functional module generates request packets for implementing memory access operations, each request packet having an operation field comprising eight bits of which a packet type bit denotes the type of the packet, four operation family bit denote the function to be implemented by the packet and three operation qualifier bits act to qualify the function.

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